Listing of Claims:

Claims 1-4 (Canceled).

5. (Currently Amended): An optimized bus connection for acceptance of bus transactions, provided with a first store operating according to a FIFO principle, in which ~~transaction processes~~ bus transactions arriving from a higher-level processor system ~~present at a higher level~~ for execution by the optimized bus connection are temporarily stored in ~~a sequence of the arriving transaction processes~~ their sequence of arrival, ~~wherein,~~ the optimized bus connection comprising:

~~following the first store, there is provided~~ a first functional section coupled to an output of the first store for classifying ~~reading out, classifying, and typifying~~ the bus transactions temporarily stored in the first store, and including means for classifying ~~by means of the first functional section~~ those transactions that must be executed in a strictly logical sequence ~~can be grouped respectively~~ as a first class of transactions, and those transactions that do not have to be executed in a strictly logical sequence ~~can be grouped respectively~~ as a second class of transactions,

~~following the first functional section, there is provided~~ a second functional section ~~with a plurality of~~ coupled to an output of said first functional section and comprising at least first and second functional lines disposed in parallel, ~~of which at least one functional line is allocated respectively to one of the two classes of transactions, by means of the first functional section, depending on the result of its classification and typification of the transactions, the bus transactions can be allocated to one of the functional lines of the second functional section. a~~ wherein said first functional line is allocated to the first class of transactions, and is provided with a storage structure functioning according to the FIFO principle, ~~a further~~ and wherein said second functional line is allocated to said second class of transactions, and has a storage structure suitable for random accesses, and

~~following the second functional section, there is provided~~ a third functional section with an execution unit ~~common~~ coupled to the functional lines of the second functional section, ~~by means of which~~ and comprising means for organizing the transactions ~~contained in the individual function~~ allocated to said at least first and second functional lines of the second functional section ~~can be organized~~ into a serial sequence for forwarding to the higher-level processor system, ~~present at a higher level, and~~

wherein the organizing means of said execution unit ~~is configured to move~~ moves a transaction of the second class ahead of a transaction of the first class, depending on a state of the higher-level processor system.

6. (Currently Amended): An optimized bus connection according to Claim 5, wherein,

~~for~~ the second class of transactions includes read and write types, ~~there is provided in~~

the first functional section typifies the bus transactions temporarily stored in the first store, and

the second functional section ~~on a basis of division of transactions into two types, which are read and write transactions, an independent functional line~~ includes a respective one of said at least first and second functional lines for each of said types.

7. (Currently Amended): An optimized bus connection according to Claim 5, wherein [[,]]

~~for~~ a first shortcut bypasses said first store, said first functional section and said second functional section so that bus transactions ~~starting from the bus connection up to~~ arrive at the execution unit of the third functional section[[,]] ~~there is implemented~~ from the higher-level

processor system by means of [[a]] said first shortcut which operates on condition that an empty state exists in the ~~first two~~ first and second functional sections.

8. (Currently Amended): An optimized bus connection according to Claim 6, wherein[[,]]

~~for~~ a first shortcut bypasses said first store, said first functional section and said second functional section so that bus transactions ~~starting from the bus connection up to~~ arrive at the execution unit of the third functional section[[,]] ~~there is implemented~~ from the higher-level processor system by means of [[a]] said first shortcut which operates on condition that an empty state exists in the ~~first two~~ first and second functional sections.

9. (Currently Amended): An optimized bus connection according to Claim 5, wherein[[,]]

~~for~~ a second shortcut bypasses said first functional line so that at least one transaction of the first class of transactions[[,]] ~~starting from a point of arrival in the second functional section up to~~ arrives at the execution unit of the third functional section[[,]] ~~there is implemented~~ from the first functional section by means of [[a]] said second shortcut which operates on condition that an empty state exists in the first functional line ~~allocated to the first class~~.

10. (Currently Amended): An optimized bus connection according to Claim 6, wherein[[,]]

~~for~~ a second shortcut bypasses said first functional line so that at least one transaction of the first class of transactions[[,]] ~~starting from a point of arrival in the second functional section up to~~ arrives at the execution unit of the third functional section[[,]] ~~there is implemented~~ from the first functional section by means of [[a]] said second shortcut which operates on condition that an empty state exists in the first functional line ~~allocated to the first class~~.

11. (Currently Amended): An optimized bus connection according to Claim 7, wherein[[,]]

~~for~~ a second shortcut bypasses said first functional line so that at least one transaction of the first class of transactions[[,]] ~~starting from a point of arrival in the second functional section up to~~ arrives at the execution unit of the third functional section[[,]] ~~there is implemented~~ from the first functional section by means of [[a]] said second shortcut which operates on condition that an empty state exists in the first functional line ~~allocated to the first class~~.

12. (Currently Amended): An optimized bus connection according to Claim 8, wherein[[,]]

~~for~~ a second shortcut bypasses said first functional line so that at least one transaction of the first class of transactions[[,]] ~~starting from a point of arrival in the second functional section up to~~ arrives at the execution unit of the third functional section[[,]] ~~there is implemented~~ from the first functional section by means of [[a]] said second shortcut which operates on condition that an empty state exists in the first functional line ~~allocated to the first class~~.